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L30: Entry 1 of 1 File: USPT Jul 7, 1998

DOCUMENT-IDENTIFIER: US 5777399 A
TITLE: Portable electronic apparatus and charge controlling method for portable electronic apparatus

Brief Summary Text (16):
The portable electronic apparatus may be constructed such that the slow charging means includes two slow charging circuits having different output electric current values, and the CPU has a controlling function for switching the two slow charging circuits in response to an on or off state of the power supply switch detected by the open/close detection means upon slow charging.

CLAIMS:

2. A portable electronic apparatus as claimed in claim 1, wherein

said slow charging means includes two slow charging circuits having different output electric current values, and

said CPU having a controlling function for switching said two slow charging circuits in response to an on or off state of said power supply switch detected by said open/close detection means upon slow charging.

L28: Entry 1 of 4 File: USPT Dec 15, 1998

DOCUMENT-IDENTIFIER: US 5850156 A
TITLE: Processor supervisory circuit and method having increased range of power-on reset signal stability

Abstract Text (1):
For use in a processor supervisory circuit, a power-on reset circuit, a method of producing a power-on reset ("RESET") signal and a power supply including the circuit. The circuit includes: (1) an adaptive, nonlinear voltage divider having a voltage input and a voltage output, the divider dividing an unscaled, unregulated voltage received at the voltage input by a factor that varies a function of the unscaled, unregulated voltage to produce a scaled, unregulated voltage at the voltage output and (2) a comparison circuit for comparing the scaled, unregulated voltage with a scaled, regulated voltage to produce the RESET signal when the scaled, regulated voltage exceeds the scaled, unregulated voltage, the divider being adaptive and nonlinear to ensure that the comparison circuit continuously produces the RESET signal when the scaled, regulated voltage exceeds the scaled, unregulated voltage and thereby avoid premature activation of a processor couplable to the power-on reset circuit.

Current US Original Classification (1):
327/143

Current US Cross Reference Classification (1):
327/198

L28: Entry 2 of 4 File: USPT Nov 3, 1998

DOCUMENT-IDENTIFIER: US 5831849 A
TITLE: Data control system

Abstract Text (1):
In a data control system according to the present invention, a data storage unit such as a memory or a register of each slave apparatus receives supply of power from a first power source which supplies power to a master apparatus, and is separated from a second power source which supplies power to different circuits of the slave apparatus except the data storage section. A CPU of the master apparatus has a function of discriminating operation conditions of the two first and second power sources and controlling initialization of the slave apparatus including the data storage units and the other circuits. Each of the slave apparatus includes a first power-on reset circuit for detecting power-on of the first power source and outputting an initialization reset signal for the data storage unit, and a second power-on reset circuit for detecting power-on of the second power source and outputting an initialization reset signal of the circuits other than the data storage unit.

Current US Cross Reference Classification (4):
714/22

L28: Entry 3 of 4 File: USPT Sep 20, 1994

DOCUMENT-IDENTIFIER: US 5349695 A
TITLE: Selective call receiver having CMOS power-on reset circuit

Abstract Text (1):
A selective call receiver (100) operates to recover an information signal and is capable of receiving a battery supplying a first voltage (203) that is multiplied to generate a second voltage (212). The selective call receiver (100) includes [comprises] a processor (106) that extracts message information contained within the recovered information signal for presentation and a power-on reset circuit (112) that generates a power-on reset signal having [comprising] first and second portions corresponding with a processor reset and a processor execute state, respectively. The power-on reset signal changes from the processor reset to the processor execute state when the second voltage (212) exceeds a sum of a PMOS threshold voltage and a NMOS threshold voltage, thereby completing a power-on reset of the processor (106).

Current US Cross Reference Classification (1):
327/143

L11: Entry 1 of 10 File: USPT Dec 23, 2003

DOCUMENT-IDENTIFIER: US 6667764 B1
TITLE: Video camera apparatus and video monitor system

Detailed Description Text (6):
The video camera apparatus includes a microprocessor 17 for controlling respective circuits of the video camera apparatus 31, an EPROM (Electrically programmable read-only memory) 4 for storing programs for predetermined operations, an EEPROM (Electrically erasable programmable read-only memory) 5 for storing data, such as historic data, a data communication circuit 1 for communicating with the monitor site 32 through a cable or a network, a power supply 2 for supplying powers to respective circuits of the video camera apparatus 31, a power-on reset circuit 28 for detecting turning on of the power to inform the microprocessor 17 of the power on, a video camera unit 33 for receiving an image around the video camera apparatus 31 and generates an image signal, a video signal processor 3 for processing the image signal from the imaging circuit 15 to generate a video signal from the image signal and transmitting the video signal to the monitor site 32, a tilting unit 26 for tilting the video camera unit 33, a panning unit 27 for panning the video camera 33, a sensor unit 35 for detecting conditional data around the video camera apparatus 31 and sending the conditional data to the microprocessor 17, a counter 16 for counting the number of times of preset operations, and a time measuring circuit 18 for a measuring time interval of the preset operation and generating a time clock signal indicative of the present time.

L11: Entry 2 of 10 File: USPT Oct 14, 2003

DOCUMENT-IDENTIFIER: US 6633202 B2
TITLE: Precision low jitter oscillator circuit

Detailed Description Text (28):
The interface/system controller 42 is coupled between a serial data interface pin 12M on the IC 12, and the sound processor 38. This interface is used to communicate with an external controller for the purpose of setting the parameters of the system. These parameters can be stored on-chip in the EEPROM 44. If a "black-out" or "brown-out" condition occurs, then the power-on reset circuit 46 can be used to signal the interface/system controller 42 to configure the system into a known state. Such a condition can occur, for example, if the battery fails.

L11: Entry 3 of 10 File: USPT Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414905 B1
TITLE: Method and apparatus for communicating coded messages in a wellbore

Detailed Description Text (94):
Latches 247, 249 are utilized as one bit memory devices which record the origin of the event which results in power being provided to microprocessor 255. If the ONP terminal of latch 249 is high, a change in pressure, as detected by pressure change detection circuit 237, caused power to be provided to microprocessor 255. If the ONU terminal of latch 247 is high, the receipt of a binary character at magnetic communication interface circuit 115 caused power to be provided to microprocessor 255. As can be seen from FIG. 12, the ONP terminal and the ONU terminal are provided as inputs to or-gate 253. If either one of the ONP terminal or the ONU terminal go high, or-gate 253 goes high, causing the closure of electrically-actuated switch 269 which results in five volts being applied to the reset input pin of microprocessor 255. Simultaneously, power-on reset circuit 251 is utilized to provide power to the power input of microprocessor 255.

L11: Entry 4 of 10 File: USPT Feb 5, 2002

DOCUMENT-IDENTIFIER: US 6343744 B1
TITLE: Noncontact type IC card and system therefor

Detailed Description Text (6):
FIG. 2 shows the IC card 8. As shown in FIG. 2, the IC 2 has a resonance capacitor 2a, full-wave rectification circuit 2b, smoothing capacitor 2c, clock generation circuit 2d, constant voltage circuit 2e, demodulation circuit 2f, modulation circuit 2g, power-on reset circuit 2h, and digital circuit 2i. The digital circuit 2i has a ROM, RAM, or nonvolatile memory in addition to a CPU, and further includes a co-processor, clock generator, initial response protocol control circuit, interface circuit for asynchronous communication with an analog section, and the like, as needed. When an electromagnetic field radiated from the external read/write device is tuned by the resonance capacitor 2a, a voltage is induced by the antenna 4. The voltage induced by the antenna 4 is rectified by the full-wave rectification circuit 2b, smoothed by the smoothing capacitor 2c, and supplied to the constant voltage circuit 2e or demodulation circuit 2f. The constant voltage circuit 2e generates a predetermined voltage VDD and supplies it to the digital circuit 2i. The demodulation circuit 2f demodulates a received signal and supplies it to the digital circuit 2i. The clock generation circuit 2d generates a clock CLK from the voltage induced by the antenna 4 and supplies the clock CLK to the digital circuit 2i. The power-on reset circuit 2h monitors the clock generated by the clock generation circuit 2d, the constant voltage output from the constant voltage circuit 2e, and the outputs from the demodulation circuit 2f and modulation circuit 2g. The power-on reset circuit 2h determines on the basis of the monitor result whether sufficient power for the operation of the digital circuit 2i is supplied, and sends a reset signal for the start of driving to the digital circuit 2i. The digital circuit 2i is driven in synchronism with the clock CLK and operated on the basis of the signal supplied from the demodulation circuit 2f. Hence, a signal supplied from the external read/write device is processed by the digital circuit 2i. The digital circuit 2i can also transmit a signal to the external read/write device and transmits information through the modulation circuit 2g and antenna 4.

L11: Entry 5 of 10 File: USPT Dec 12, 2000

DOCUMENT-IDENTIFIER: US 6160431 A
TITLE: Power-on reset circuit for dual supply voltages

Brief Summary Text (8):
Some microprocessors and programmable devices, such as field programmable gate arrays and programmable logic devices, use a first supply voltage Vcc1 for input/output logic circuits and a second supply voltage Vcc2 for internal logic circuits. Typically, transistors using lower supply voltages are able to switch logic levels at a faster rate. However, input/output logic circuits may require higher supply voltages to communicate to other IC devices on printed circuit boards. Thus, the Vcc1 target voltage for the input/output logic circuits is typically greater than the Vcc2 target voltage for the internal logic circuits. When a circuit is partly powered up, second supply voltage Vcc2 may be adequate, while first supply voltage Vcc1 may be inadequate. Under these conditions, the logic circuits which receive first supply voltage Vcc1 and provide signals to the logic circuits which receive second supply voltage Vcc2 would provide erroneous signals. Therefore, even the logic circuits which receive second supply voltage Vcc2 are likely to produce erroneous results. Thus, on IC devices with multiple supply voltages, there is a need for a power-on reset circuit to reset logic circuits which use a second supply voltage if a first supply voltage becomes inadequate.

L11: Entry 7 of 10 File: USPT Jul 13, 1999

DOCUMENT-IDENTIFIER: US 5923264 A
TITLE: Multiple access electronic lock system

Detailed Description Text (11):
The lock controller 76 includes a switch interface 94 that clears the memory of the microprocessor 86 and initiates a program mode by use of a reset switch 96 and an initiate program switch 98. The microprocessor 86 and various functions are synchronized by an oscillator 100. A power-on reset circuit 102 also provides an input to the microprocessors 86 to commence the operating mode. A real-time clock and audit trail memory 104 communicate with the microprocessor to record the chronological history of each attempted lock/unlock event and the associated access code entered. A privacy button 106 mounted to the rear assembly and accessible at the secured side of the door can also be included to prevent actuation of the lock from the exterior side regardless of the input entered at the readers 42, 44.

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L3: Entry 3 of 3 File: TDBD Jul 1, 1994

DOCUMENT-IDENTIFIER: NN9407529
TITLE: Optical Link Control Protocol for Remote Apparatuses with Automatic Power On/Off Function

Disclosure Text (1):
Disclosed is a method to turn on/off the power of remote apparatuses which are connected to a main system unit via optical links. The principle of the method is that the power of the remote apparatus is kept turned on if and only if the apparatus is receiving valid communication data on the link. No explicit commands to control the remote power is necessary but a stand-by power supply for the receiver in the remote apparatus is assumed. - It is a very common demand to turn on/off the power of apparatuses located at a distant place in response to a main system unit. A conventional approach is to equip a copper line along with a communication link to the remote apparatus, with which a relay for the remote power is turned on/off. Although the simplicity of the conventional approach, it does not fit to the recently proliferating optical communication links. A simple durable protocol for these optical links without using a copper line is proposed. - Suppose the optical link uses a synchronous communication method, that is, the data over the link is encoded in a certain way and filler codes are padded during no meaningful data is transferred from the main unit. Also suppose a stand-by power supply is equipped to the receiver circuit of the optical link at the remote side and the main power for the remote apparatus is turned on/off with this link controller. Power-On Sequence: 0) At first the main unit is not turned on and no valid codes are transmitted to the remote side. The receiver at the remote side is in a stand-by state and always verifying the receiving data. Since the received data is not valid codes, the main power of the remote unit is not turned on. - 1) When the main unit is turned on, it begins to send valid communication codes to the remote side. The receiver at the remote side verifies the codes for a certain duration and then turns on the main power of the remote apparatus. If the verification is not satisfied, it remains in the stand-by state. - 2) After the main power of the remote apparatus is turned on, the link controller at the remote side begins to send valid communication codes to the main unit. The receiver of the main unit verifies them for a certain duration and then recognizes the remote apparatus successfully turned on. Power-Off Sequence: 0) The filler codes are padded during no meaningful data is transmitted over the link and the receivers at both ends always verify those codes on the link. If the remote side detects errors such as invalid code, wrong sequence of codes and time-out of hand-shake communication, two situations must be taken into account; one is the main unit is turned off and no more valid codes come; the other is the link is in a tentative trouble like electromagnetic interference and should be recovered soon. - 1) When the remote side receiver detects an error on the link, it sends an error information to the main unit and then gets into a ready-to-power-off state. It stays in the state for a certain duration which is longer enough than the length of the error recovery sequence stated in 2). As long as it receives the filler codes at a significant ratio, it stays in the state. - 2) When the link controller at the main unit receives the error information from the remote side, it issues a non-maskable interrupt to the processor of the main unit. If the error is a communication error and the link should be recovered, the interrupt handler goes

through an error recovery sequence and the controller restarts to send valid codes again. The controller keeps sending the filler codes during this. On the other hand, if the error is caused by a voltage drop at the sender circuit of the main unit according to its power-off, no handling nor recovery is necessary. - 3) If the remote side receiver begins to receive valid codes other than filler codes again, the state of the remote link controller gets back to the normal state without turning off the main power of the remote apparatus. If it does not receive valid codes including filler codes at the ratio for the duration stated in 1), it turns off the main power of the remote apparatus and gets into the stand-by state. - Since automatic gain control circuits are used at the receiver circuits of optical links, phantom data patterns are generated at the receivers from the environmental light or thermal noise when the sender does not send any light. Because of this phantom patterns, the verification time on the validity of the codes is necessary to turn on/off the main power. - With this method, neither explicit communication commands nor programs to control the power is necessary. - Furthermore, if the on/off-response time of the main power of the remote apparatus is slow enough, the link controller of the remote apparatus does not need a power-on-reset signal at the very initial power-on time of its stand-by power. The controller might start from any internal state but the power-off sequence described above conducts to the single stand-by state. Since the on/off-response is slow, the power supply does not response to this tentative abnormal state of the controller.

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L3: Entry 2 of 3 File: JPAB Mar 25, 1986

DOCUMENT-IDENTIFIER: JP 61058020 A
TITLE: INITIALIZING SYSTEM

Abstract Text (2):
CONSTITUTION: An automatic power supply controller 10 actuating a power supply circuit 15 of a central processor gives an inquiry signal to each I/O 6 to sense the power ON state. When a response exists, the controller 10 activates the power supply circuit 15 to turn on the power of the central proces sor. In this case, a communication line 5 with the I/O 6 is connected to the central processor from the controller 10 by a changeover switch to attain data transmission/reception. In this case, a generating circuit 11 of a periodical initial izing signal is provided in addition to the generating circuits 3, 4 for a forced initializing signal by the external command and for the initializing signal at application of power as the reset means of the controller 10 and the initializing signal is inputted in parallel with the OR circuit 2. Thus, a reset signal is given to the controller 10 at a prescribed period and the system inactivation due to the runaway of the controller 10 is prevented.

L4: Entry 1 of 11 File: USPT May 4, 2004

DOCUMENT-IDENTIFIER: US 6731258 B2
TITLE: Fast-working LCD residual display suppression circuit and a method thereto

Brief Summary Text (13):
The fast-working residual display suppression circuit for LCD includes: a manual selector for outputting a manual control signal; an automatic detection circuit for automatically detecting the power state and output an automatic control signal; a selection switch for eliminating residual display and outputting an activating signal according to either the manual signal or the automatic signal; a signal level conversion circuit for receiving the activating signal and producing the desired voltage level output; a fast discharge circuit for quickly eliminating LCD residual display based on the activating signal and the desired voltage level output; and an LCD power controller for cutting off the power supplied to the fast discharge circuit based on the activating signal to speed up the discharge rate.

L4: Entry 4 of 11 File: USPT Jan 28, 2003

DOCUMENT-IDENTIFIER: US 6512511 B2
TITLE: Hand grippable combined keyboard and game controller system

Detailed Description Text (15):
Although not shown, each of housings 102 and 104 includes a battery compartment which contains the power source for operation of the circuitry associated with converting the switch closures to particular computer input signals. Such batteries may be of the rechargeable type, in which case a charging jack is also installed and accessible external to the housing 102, 104. Also not shown, is a power switch associated with each housing 102, 104 to enable the circuits thereof. Such a switch may be provided at any convenient location or functionally provided by means of automatic circuitry known in the art, which "turns off" the circuitry associated with a particular housing 102, 104 after a particular time period of non-use. Such automatic power control may be triggered to the "power on" state by the physical displacement of the housing 102, 104, as sensed by a position sensitive switch, such as a mercury switch, or alternately by actuation of any of the switches carried by the particular housing.

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L8: Entry 1 of 1 File: USPT Oct 31, 2000

DOCUMENT-IDENTIFIER: US 6141764 A
** See image for Certificate of Correction **
TITLE: Method for initializing an electronic device using a dual-state power-on-reset circuit

Abstract Text (1):
An initializer that responds to change in a power supply potential level, for generating an initialize signal to initialize a circuit to a select state, the initializer includes a power-on reset circuit that switches between an active and a powered-down state, and is for generating the initialize signal. The initializer also includes a wake-up circuit that monitors the power supply potential level and switches the power-on reset circuit from the powered-down state to the active state when selected change in the power supply potential level occurs.

Brief Summary Text (12):
The present invention overcomes the above identified problems as well as other shortcomings and deficiencies of existing technologies by providing circuitry to detect change in a power supply potential level and to switch a power-on reset circuit from a powered-down state to an active state, while maintaining minimum power consumption.

Brief Summary Text (14):
It is a further object of the present invention to provide an initializer having a power-on reset circuit that switches between a powered-down state and an active state when change in a power supply potential level is detected.

Brief Summary Text (16):
There is further provided an initializer that is operable in response to change in a power supply potential level, that generates an initialize signal to initialize a circuit to a selected state. The initializer includes a power-on reset circuit that generates the initialize signal and is switchable between a stand-by state and an active state. The initializer also includes a detector that detects the change in the power supply potential level and includes a signal generator that generates a wake-up signal when change in the power supply potential level is detected. The wake-up signal switches the power-on reset from the stand-by state to the active state.

Detailed Description Text (3):
Initializer 114 includes a power-on reset (POR) circuit 116 connected to a wake-up circuit 118. It is preferred that POR circuit 116 be a power-on reset circuit having a stand-by state, and an active state wherein when in the stand-by state, power consumption by the POR circuit can be minimized.

CLAIMS:

1. A method for initializing an electronic device, the method comprising the steps of:

detecting a change in a power supply voltage;

generating a signal to switch a power-on-reset (POR) circuit from a first power state to a second power state responsive to detecting a change in the power supply voltage;

determining if the power supply voltage has fallen below a minimum operating voltage; and

responsive to the determination that the power supply voltage has fallen below the minimum operating voltage, generating an initialization signal for the electronic device.

4. The method of claim 1, wherein the step of generating a signal to switch the POR circuit comprises the step of:

generating a signal to switch the POR circuit from a stand-by power state to an active power state responsive to detecting a change in the power supply voltage.